OMB No. 0651-0011

INFORMATION DISCLOSURE CITATION

Atty. Docket No.	0673.0070-00	Serial No.	10/062,714
Applicant	Ming-Dou KER, et al.		
Filing Date	February 5, 2002	Group:	2811

U.S. PATENT DOCUMENTS

Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
VAMJ		5,910,874	06/08/1999	Iniewski et al.			
VAMJ		5,646,808	07/08/1997	Nakayama			
VAMJ		5,519,242	05/21/1996	Avery			
VAMJ		5,631,793	05/20/1997	Ker et al.			
VAMJ		5,811,857	09/22/1998	Assaderaghi et al.			
VAMJ		5,502,328	03/26/96	Chen et al.			
VAMJ		5,581,104	12/03/96	Lowrey et al.			
VAMJ		5,990,520	11/23/99	Noorlag et al.			

FOREIGN PATENT DOCUMENTS

		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

VAMJ	M-D. KER, et al., "CMOS On-Chip ESD Protection Design with Substrate-triggering Technique," Proc. of ICECS, Vol. 1, pp. 273-276, 1998
VAMJ	C. Duvvury et al., "Dynamic Gate Coupling for NMOS for Efficient Output ESD Protection", Proc. of IRPS, pp. 141-150, 1992

Examiner	Victor A. Mandala Jr	Date Considered	12-13-02

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U.S. PATENT DOCUMENTS

Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
VAMJ		5,907,462	05/25/99	Chatterjee et al.			
VAMJ		5,932,918	08/03/99	Krakauer			
VAMJ		6,015,992	01/18/00	Chatterjee et al.			
VAMJ		5,453,384	09/26/95	Chatterjee			

FOREIGN PATENT DOCUMENTS

		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

VAMJ	N. K. Verghese and D. Allstot, "Verification of RF and Mixed-Signed Integrated Circuits for Substrate Coupling Effects", in *Proc. of IEEE Custom Integrated Circuits Conf.*, 1997, pp. 363-370
VAMJ	M.Xu, D. Su, D. Shaeffer, T.Lee, and B. Wooley, "Measuring and Modeling the Effects of Substrate Noise on LNA for a CMOS GPS Receiver, "*IEEE Journal of Solid-State Circuits*, vol. 36, pp. 473-485, 2001.
VAMJ	R. Gharpurey, "A Methodology for Measurement and Characterization of Substrate Noise in High Frequency Circuits," in *Proc. of IEEE Custom Integrated Circuits Conf.*, 1999, pp. 487-490.
VAMJ	M. Nagata, J. Nagai, K. Hijikata, T. Morie, and A. Iwata, "PhysicalDesign Guides for Substate Noise Reduction in CMOS Digital Circuits, "*IEEE Journal of Solid-State Circuits*, vol. 36, pp. 539-549, 2001.
VAMJ	M.-D. Ker, T-Y, Chen, C-Y. Wu, and H.-H. Chang, "ESD Protection Design on Analog Pin WIth Very Low Input Capacitance for High-Frequency or Current-Mode Applications, "*IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1194-1199, 2000.
VAMJ	M.-D. Ker, "Whole-Chip ESD Protection Design with Efficient VDD-to-VSS ESD Clamp Circuit for Submicron CMOS VLSI, "*IEEE Trans. on Electron Devices*, vol. 46, pp. 173-183, 1999

Examiner	Victor A. Mandala Jr	Date Considered	12-13-02

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U.S. PATENT DOCUMENTS

Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
VAMJ		6,081,002	06/27/2000	Amerasekera et al			
VAMJ		5,754,381	05/19/1998	Ker			
VAMJ		5,465,189	11/07/1995	Polgreen et al.			
VAMJ		5,225,702	07/06/1993	Chatterjee			
VAMJ		5,012,317	04/30/1991	Rountre			
VAMJ		4,939,616	07/03/1990	Rountree			

FOREIGN PATENT DOCUMENTS

		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

VAMJ	C. Richier, P. Salome, G. Mabboux, I. Zaza, A. Juge, and P. Mortini, "Investigation on Different ESD Protection Strategies Devoted to 3.3V RF Applications (2 (GHz) in a 0.18μm CMOS Process, "in Proc. of EOS/ESD Symp., 200, pp. 251-259.
VAMJ	T.-Y. Chen and M.-D. Ker, "Design on ESD Protection Circuit With Low and Constant Input Capacitance," *in Proc. of IEEE Int. Symp. on Quality Electronic Design, 2001*, pp. 247-247.
VAMJ	M.-D. Ker, T.-Y. Chen, C.-Y. Wu, and H.-H. Chang, "ESD Protection Design on Analog Pin WIth Very Low Input Capacitance for RF or Current-Mode Applications, "*IEEE Journal of Solid-State Circuits*, Vol. 35, pp. 1194-1199, 2000.

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U.S. PATENT DOCUMENTS

Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
VAMJ		5,629,544	05/13/97	Voldman et al.			
VAMJ		6,034,397	03/07/00	Voldman			
VAMJ		5,940,258	08/17/99	Duvvury			
VAMJ		5,807,791	09/15/98	Bertin et al			
VAMJ		5,719,737	02/17/98	Maloney			
VAMJ		5,654,862	08/05/97	Worley et al.			

FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

VAMJ	S.Voldman, et al. , "Semiconductor Process and Structural Optimization of Shallow Trench Isolation-Defined and Polysilicon- Bound Source/Drain Diodes for ESD Networks," in Proc. of EOS/ESD Symp., 1998, pp. 151-160
VAMJ	S. Voldman, et al., "Analysis of Snubber-Clamped Diode-String Mixed Voltage Interface ESD Protection Network for Advanced Microprocessors," in Proc. of EOS/ESD symposium, 1995, pp. 43-61.
VAMJ	M.J. Pelgrom, et al., "A 3/5 V Compatible I/O Buffer," IEEE Journal of Solid-State Circuits, vol.30, no. 7, pp.823-825, July 1995.
VAMJ	G.P. Singh, et al., "High-Voltage-Tolerant I/OBuffers with Low-Voltage CMOS Process," IEEE Journal of Solid-State Circuits, vol.34, no. 11, pp. 1512-1525, Nov. 1999.
VAMJ	H. Sanchez, et al., "A Versatile 3.3/2.5/1.8-V CMOS I/O Driver Built in 02. -µm, 3.5-nm Tox, 1.8 -V CMOS Technology, " IEEE Journal of Solid-State Circuits, vol.34 no. 11.pp. 1501-1511, Nov. 1999

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